PATENT APPLICATION

PCT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	
	)	
HANSEN et al.	)	Group Art No. TBA
	)	
Serial No: 10/550,094	)	Examiner: TBA
	)	
Filed: September 21, 2005	)	Docket No. 006559.00009

For: *LIST OUTPUT VITERBI DECODER WITH BLOCKWISE ACS AND TRACEBACK*

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner of Patents
U.S. Patent and Trademark Office
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Submitted herewith is Form PTO-1449 listing documents cited earlier in an Information Disclosure Statement filed with the above-identified application. Copies of the identified references listed therein are now enclosed. It is respectfully requested that the Examiner make his/her consideration of each of these documents formally of record.

Since this Supplemental Information Disclosure Statement is being filed within 3 months of the filing date of this application and before issuance of a first Office Action on the merits under 37 C.F.R. 1.97(b), it is submitted that no fee or certification is required. However, if a fee is required, please charge our deposit account no. 19-0733.

Respectfully submitted,

Date: Nov. 2, 2005

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.H./

USPTO Form 1449 U.S. Department of Commerce
Patent and Trademark Office

INFORMATION DISCLOSURE CITATION

Sheet 1 of 1

Date of this IDS: November 2, 2005

Attorney Docket No.	Serial No.
006559.00009	TBA
Applicant(s): HANSEN et al	
Filing Date: September 21, 2005	Group: TBA

U.S. PATENT DOCUMENTS

Examiner Initial	Patent No.	Date	Name	Class	Subclass	Filing Date (if appropriate)

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Country	Class	Subclass	Translation YES	Translation NO
	GB 2 305 827 A	16 April 1997	Great Britain				

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

	CZAJA et al.: "Variable data rate Viterbi decoder with modified LOVA algorithm", TENCON '95, PROCEEEDINGS OF THE IEEE REGION 10 INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND VLSI, Hong Kong, November 6-10, 1995, pages 472-475. XP010160164.
	BOUTILLON et al.: "VLSI architectures for the MAP Algorithm", IEEE TRANSACTIONS ON COMMUNICATIONS, vol. 51, no. 2, February 2003, pages 175-185, XP001164390.
	FETTWEIS et al.: "Feedforward Architectures for Parallel Viterbi Decoding", JOURNAL OF VLSI SIGNAL PROCESSING SYSTEMS FOR SIGNAL, IMAGE, AND VIDEO TECHNOLOGY, Vol. 3, Nos. 1 / 2, June 1, 1991, pages 105-119, XP00228897.

EXAMINER /Syed Haider/ (12/14/2010) DATE CONSIDERED 12/14/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.H./